A DPLL-based per Core Variable Frequency Clock Generator for an Eight-Core POWER7™ Microprocessor

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Abstract

A per-core clock generator for the eight-core POWER7™ processor is implemented with a digital PLL. This frequency generator is capable of smooth, controlled frequency slewing, minimizing the impact of di/dt. Frequency can be dynamically adjusted while the clock is running, and without skipping any cycles, thus enabling aggressive power management techniques.

Introduction

As the number of cores in modern processors keeps growing, power management at the core level is becoming increasingly important. One common method used to trade off power against performance is changing the clock frequency of the processor [1]. Due to time dependent variations in load for a single core and across multiple cores, dynamically adjustable, per core clock generators are highly desirable. Such circuits, to be practical in a real system environment, must have low area and power overhead. Moreover, to extract the full value of per core dynamic frequency synthesis capability, it must be possible to change the frequency while the core is executing code. This drives a set of requirements for the variable frequency generator: a near-continuous set of achievable output frequencies; a controllable frequency slew rate with no skipped cycles, limiting the power supply drop caused by di/dt; and no short cycles, preventing timing hazards. In this paper we present a variable frequency generation circuit integrated in each of the eight cores in the POWER7™ processor [2], which meets all the requirements given above.

Architecture

The variable frequency generator is built around a fractional-N DPLL [3]. Figure 1 shows the top-level block diagram of the circuit. The key components of the DPLL-based generator include a bang-bang, self-timed phase and frequency detector (PFD), a digital loop filter, a digitally controlled oscillator (DCO), prescalers, a multi-modulus feedback divider together with a delta-sigma modulator, and a multiplier filter.

The output frequency of the DPLL can be changed dynamically by controlling the modulus of the feedback divider. The multiplier filter’s function is to generate a sequence of modulus values resulting in a controlled, programmable frequency slew rate. The multiplier filter block diagram is shown in Figure 2. When a new target frequency multiplier Mult_in and frequency slew rate Mult_slew are programmed into the filter, a linear sequence of multipliers

Measurements

We show in Figure 4 measurements of the well controlled frequency transient from the variable clock generator integrated within a POWER7™ core, for three different settings of the slew rate. Figure 5 shows the final piece of the transient, where three distinct regions are clearly identifiable: frequency acquisition, phase acquisition, and phase lock. In the frequency acquisition region, the generator output follows the frequency multiplier ramp. Every time that a cycle slip occurs between the reference and the feedback clock, the output frequency is changed by about 30 MHz. Once the frequency multiplier is stable, and the generator output is close to the target frequency, cycle slips stop occurring. In this phase acquisition region, the final phase and frequency are attained
using the integrator in the DPLL loop filter. Proper selection of DPLL loop filter constants ensures that no overshoot or undershoot in cycle time is present in the transient. The demonstrated combination of the controlled frequency slew rate and the absence of short cycles proves that the proposed DPLL-based variable frequency generator can be used to dynamically adjust the frequency while the core is executing code.

The DCO has a measured tuning range from 800 MHz to 12 GHz over PVT. The DCO output is divided by two to improve the duty cycle of the clock provided to the processor core logic. RMS period jitter is 1 ps at 5 GHz, and 6 ps at 1 GHz. The DPLL has an area of 200 μm x 350 μm, half of which is occupied by the voltage regulator for the DCO. Figure 6 shows a micrograph of the POWER7™ core, with the size and position frequency generator outlined.

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References