A method includes embedding high-z oxide nanoparticles in a semiconductor package of a semiconductor packaged assembly, wherein the high-z nanoparticles are operative to emit electron radiation when exposed to a radiation source to render a semiconductor device in the semiconductor package inoperable.

20 Claims, 1 Drawing Sheet
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HIGH-Z OXIDE NANOPISTLES EMBEDDED IN SEMICONDUCTOR PACKAGE

BACKGROUND

Preventing unauthorized use of semiconductor chips (integrated circuit devices or semiconductor devices) is critical to meeting certain types of government regulations. By way of example, some chips can be used for both commercial and military applications. It is understood that chips built for military applications are required to adhere to more stringent operational standards (military standards) than chips built for commercial applications. As a result, chips that are built for both commercial and military applications may not satisfy all necessary military standards. Thus, government regulations may require that such dual application chips only be sold for commercial use, and therefore military use, such as using the dual application chips in environments that require radiation hardening, is prohibited.

SUMMARY

Embodiments provide techniques for embedding high-z oxide nanoparticles in a semiconductor package. Such methods, for example, prevent unauthorized use of semiconductor chips in environments requiring radiation hardening.

For example, in one embodiment, a method comprises embedding high-z oxide nanoparticles in a semiconductor package of a semiconductor packaged assembly, wherein the high-z nanoparticles are operable to emit electron radiation when exposed to a radiation source to render a semiconductor device in the semiconductor package inoperable.

Advantageously, embedding high-z oxide nanoparticles in a semiconductor package in accordance with embodiments of the invention creates a semiconductor packaged assembly that is self-destructive when exposed to radiation. Therefore, for example, when performing reliability testing of chips intended for use in military applications by exposing the chips under test to radiation, chips that are not fully compliant with military standards (e.g., dual application chips, as mentioned above) but are formed with embedded high-z oxide nanoparticles will be destroyed and thus prevented from being used in military environments.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1A illustrates a semiconductor die encapsulated into an integrated circuit package containing high-z oxide nanoparticles, according to an embodiment of the invention.

FIG. 1B illustrates a layer containing high-z oxide nanoparticles, according to an embodiment of the invention.

FIG. 2 illustrates the integrated circuit package of FIG. 1 exposed to radiation, according to a methodology of an embodiment of the invention.

DETAILED DESCRIPTION

Embodiments will now be described in further detail with regard to techniques for preventing the unauthorized use of semiconductor chips in environments requiring radiation hardening. It is to be understood that various layers, structures, and/or regions shown in the accompanying drawings are schematic illustrations that are not necessarily drawn to scale. In addition, for ease of explanation, one or more layers, structures, and regions of a type commonly used to form semiconductor devices or structures may not be explicit-
comprises gamma radiation. As mentioned above, the level of the radiation 205 alone may not be sufficient to permanently destroy semiconductor chip 120. However, in accordance with embodiments of the invention, semiconductor package 110 is embedded with high-z oxide nanoparticles (HIO$_2$) 115 operative to enhance the level of radiation received by semiconductor chip 120. As mentioned, the high-z oxide nanoparticles 115 may comprise HIO$_2$.

Thus, as illustrated in FIG. 2, when semiconductor packaged assembly 100 receives radiation 205, the HIO$_2$ nanoparticles emit electron radiation 210. Note that rays of radiation are illustratively depicted in the figures by the arrows. The enhanced radiation provided by the addition of the electron radiation 210 emitted by the nanoparticles 115 is sufficient to prevent operation of semiconductor chip 120 (i.e., prevent unauthorized use by permanently destroying the chip).

Semiconductor devices are affected by two basic radiation damage mechanisms: displacement damage and ionization damage. Displacement damage occurs when incident radiation displaces silicon atoms from their lattice sites. The resulting defects alter the electronic characteristics of the crystal. Ionization damage occurs when energy absorbed by electronic ionization in insulating layers, predominantly SiO$_2$, liberates charge carriers, which diffuse or drift to other locations where they are trapped, leading to unintended concentrations of charge and, as a consequence, parasitic fields. For MOSFETs, the most pronounced impact comes from ionization effects, as the key to their operation lies in the oxide that couples the gate to the channel. Positive charge buildup due to hole trapping in the oxide and at the interface shifts the gate voltage required for a given operating point to more negative values. This shift affects the operating points in analog circuitry and switching times in digital circuitry. Accordingly, the enhanced radiation provided by the addition of the electron radiation 210 emitted by the nanoparticles is sufficient to permanently destroy the semiconductor chip 120 through displacement damage and/or ionization damage.

It is to be understood that the methods discussed herein for fabricating semiconductor structures can be incorporated within semiconductor processing flows for fabricating other types of semiconductor devices and integrated circuits with various analog and digital circuitry or mixed-signal circuitry. In particular, integrated circuit dies can be fabricated with various devices such as transistors, diodes, capacitors, inductors, etc. An integrated circuit in accordance with embodiments can be employed in applications, hardware, and/or electronic systems. Suitable hardware and systems for implementing the invention may include, but are not limited to, personal computers, communication networks, electronic commerce systems, portable communications devices (e.g., cell phones), solid-state media storage devices, functional circuitry, etc. Systems and hardware incorporating such integrated circuits are considered part of the embodiments described herein.

Furthermore, various layers, regions, and/or structures described above may be implemented in integrated circuits (chips). The resulting integrated circuit chips can be distributed by the fabricator in raw wafer form (that is, as a single wafer that has multiple unpackaged chips), as bare die, or in a packaged form. In the latter case, the chip is mounted in a single chip package (such as a plastic carrier, with leads that are affixed to a motherboard or other higher level carrier) or in a multichip package (such as a ceramic carrier that has either or both surface interconnections or buried interconnections). In any case, the chip is then integrated with other chips, discrete circuit elements, and/or other signal processing devices as part of either (a) an intermediate product, such as a motherboard, or (b) an end product. The end product can be any product that includes integrated circuit chips, ranging from toys and other low-end applications to advanced computer products having a display, a keyboard or other input device, and a central processor.

Although illustrative embodiments have been described herein with reference to the accompanying drawings, it is to be understood that the invention is not limited to those precise embodiments, and that various other changes and modifications may be made by one skilled in art without departing from the scope or spirit of the invention.

What is claimed is:

1. A method comprising:

- embedding high-z oxide nanoparticles in a semiconductor package of a semiconductor packaged assembly, wherein embedding the high-z oxide nanoparticles comprises forming a layer comprising the high-z oxide nanoparticles at least one of on and in the semiconductor package, and wherein forming the layer comprises suspending the high-z nanoparticles in a solvent, and depositing the suspended high-z nanoparticles via a deposition technique;

- wherein the high-z nanoparticles emit electron radiation when exposed to radiation emitted by a radiation source to render a semiconductor device in the semiconductor package inoperable.

2. The method of claim 1, wherein the high-z oxide nanoparticles comprise HIO$_2$.

3. The method of claim 1, wherein the semiconductor package comprises a polymer package.

4. The method of claim 1, wherein radiation from the radiation source comprises gamma radiation.

5. The method of claim 1, wherein the semiconductor device comprises a silicon-on-insulator substrate-based semiconductor device.

6. The method of claim 1, wherein the semiconductor device comprises a complementary metal oxide semiconductor device.

7. The method of claim 1, wherein the deposition technique is selected from the group consisting of: spin coating, spray coating and doctor blading.

8. The method of claim 1, wherein the solvent is selected from the group consisting of: aqueous material and organic material.

9. A method comprising:

- providing a semiconductor packaged assembly comprising a semiconductor device and a semiconductor package with embedded high-z oxide nanoparticles, wherein the semiconductor package comprises a layer comprising the high-z oxide nanoparticles at least one of on and in the semiconductor package formed by suspending the high-z nanoparticles in a solvent and depositing the suspended high-z nanoparticles via a deposition technique; and

- exposing the semiconductor package to a radiation source such that, in response to radiation emitted by the radiation source, the high-z nanoparticles emit electron radiation to render the semiconductor device in the semiconductor package inoperable.

10. The method of claim 9, wherein the high-z oxide nanoparticles comprise HIO$_2$.

11. The method of claim 9, wherein the semiconductor package comprises a polymer package.

12. The method of claim 9, wherein the radiation from the radiation source comprises gamma radiation.
13. The method of claim 9, wherein the semiconductor device comprises a silicon-on-insulator substrate-based semiconductor device.

14. The method of claim 9, wherein the semiconductor device comprises a complementary metal oxide semiconductor device.

15. An apparatus comprising:
   a semiconductor device; and
   a semiconductor package having the semiconductor device contained therein; and
   a layer formed at least one of on and in the semiconductor package by suspending high-z oxide nanoparticles in a solvent and depositing the suspended high-z oxide nanoparticles via a deposition technique; wherein the high-z nanoparticles emit electron radiation when exposed to radiation emitted by a radiation source to render the semiconductor device inoperable.

16. The apparatus of claim 15, wherein the high-z oxide nanoparticles comprise HIO₃.

17. The apparatus of claim 15, wherein the semiconductor package comprises a polymer package.

18. The apparatus of claim 15, wherein radiation from the radiation source comprises gamma radiation.

19. The apparatus of claim 15, wherein the semiconductor device comprises a silicon-on-insulator substrate-based semiconductor device.

20. The apparatus of claim 15, wherein the apparatus is implemented as part of an integrated circuit.